# 3D Integration of CMOS and MEMS using Mechanically Flexible Interconnects (MFI) and Through Silicon Vias (TSV)

Hyung Suk Yang and Muhannad S. Bakir
Gigascale Integration (GSI) Group
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, Georgia, 30332
Tel: (404) 513-6864; Fax: (404) 894-0462
Email: jyang@gatech.edu

**Abstract**

A 3D integration scheme for integrating a state-of-the-art CMOS IC with an arbitrary MEMS/sensor chip is reported. The integration scheme consists of a CMOS IC and a MEMS chip stacked on top of each other with the electrical interconnections between the chips being made using mechanically flexible interconnects (MFIs). In order to expose the MEMS/sensor device to the environment for sensing, the back side of the MEMS chip is assembled to the top side of the CMOS IC, with through silicon vias (TSVs) used to route the electrical signals from the MEMS devices on top side of the chip to the back side of the chip.

Mechanically flexible interconnects are wafer-level batch fabricated interconnect structures that have high compliances in both in-plane and out-of-plane directions. The tapered interconnect design and curved beam profile allows the beam to use the 100% of the 20μm stand-off height without being damaged or undergoing a significant yielding. MFIs can be assembled using a flip-chip bonder and a key to successful bonding is the polymer ring technology that confines the solder to the tip of the MFIs during the reflow process.

The second essential component in this integration scheme is the Through Silicon Via (TSV) technology that can be fabricated in wafers that already has sensitive MEMS devices (i.e., for post-MEMS TSV fabrication); the fabrication process does not require the use of a Chemical Mechanical Planarization (CMP) process on the device side of the wafer, and the use of "mesh" membrane allows efficient seed layer formation in relatively thick MEMS wafers. In this paper, the design, the fabrication, the mechanical simulation, mechanical characterization and assembly results for MFIs are reported. Fabrication result for the TSV technology is also reported.

## I. Introduction

Three-dimensional (3D) integration of CMOS ICs and MEMS (or sensors) chips offers an enormous advantage to microsystem designers. This is because almost all MEMS chips require an interaction with a CMOS IC for processing raw signals (signal conditioning, amplification, processing, actuation, etc.) from individual MEMS devices; high density and low parasitic interconnects common to most 3D integration schemes mean that even raw signals from a large area-array of devices and sensors can be processed simultaneously in parallel using low parasitic interconnects. Such capabilities are critical for applications that require simultaneous capturing of the data from large and dense array of sensors and devices. Also, vertical integration through chip stacking means that microsystems with smaller form factor can be achieved [1, 2, 3] – an increasingly important feature as we enter the "more than Moore" era.

Unfortunately, despite the growing number of MEMS devices and processes to fabricate them [2], most of the new technologies for 3D integration of CMOS and MEMS have been developed with one specific application and one specific MEMS device in mind; as such, the developed technologies are not directly transferable to applications involving other MEMS devices. Given the large and ever growing forms of MEMS and sensor devices, what is needed is a 3D integration scheme including a set of ancillary technologies that allows arbitrary MEMS devices to be integrated with a state-of-the-art CMOS IC i.e. ancillary technologies to enable the marriage of CMOS and MEMS.

## II. CMOS and MEMS Integration Schemes

One method of integrating CMOS and MEMS is through the monolithic approach where MEMS devices are fabricated directly within the CMOS IC [4]. The CMOS process is often completed prior to the fabrication of MEMS devices and as a result, the type of processes and materials that can be used for the fabrication of MEMS devices are severely limited - in fact, one focus of the researchers in monolithic integration have been about fabricating new MEMS devices with limited materials and within the thermal process window tolerated by common CMOS processes [3]. Despite the high density and low parasitic interconnections possible with the monolithic integration, the increased complexity may make the development cost and time-to-market high and long. Because of the limited process window for the MEMS/CMOS, performance may also be compromised. Therefore, monolithic integration for a majority of MEMS/sensor products may not be the most ideal platform.

On the other end of the spectrum is the package-based

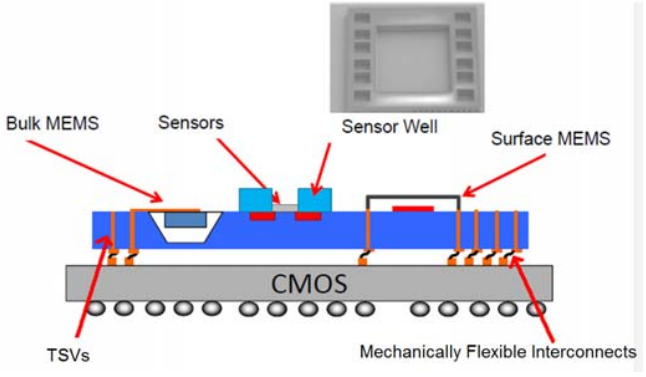


Figure 1. One potential integration scheme using mechanically flexible interconnects and through silicon vias.

 

integration (Figure 2), which is currently the most commonly used method of integrating CMOS and MEMS [3]. This is because, unlike monolithic integration, the integration method allows arbitrary MEMS chips and state-of-the-art CMOS ICs to be integrated with relative ease; CMOS ICs and MEMS chips are fabricated independently and as a result both CMOS and MEMS fabrications can be done without being limited to specific materials or processes.

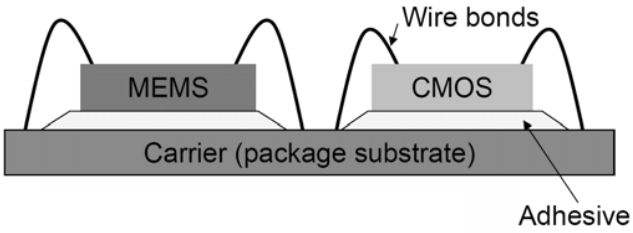


Figure 2. Package-based integration of CMOS and MEMS.

Unfortunately, as MEMS technologies advance rapidly, the demand for high density and low parasitic interconnections between MEMS devices and CMOS IC cannot be fulfilled with wirebond technology commonly used for a package-based integration. Wirebonds not only have a poor electrical performance, but its I/O density is limited by its peripheral array configuration and its inability to be batch fabricated [5]. The package-based integration with wirebonds also requires adhesives for the attaching the die to the package substrate and this method has been known to cause flexing of the MEMS die due to the thermomechanical stress [6, 7].

Flip-chip bonding is an alternative to wirebonds. Unlike the wirebonding technology, it can be batch fabricated and has a better electrical performance as well. However, a package-based integration with flip-chip bonding still remains a 2D integration and as a result, the performance is still limited by the long routing and redistribution wires on the package substrate. Flip-chip bonding, depending on substrate material and chip size, may also require the use of underfill to prevent die cracking caused by thermomechanical stress. Underfill, if needed, can potentially interfere with released MEMS structures. It has also been known to degrade RF performance at high frequencies [8]. However, even with the use of underfill, the thermomechanical stress experienced by the chip is still significant. Flip-chip bonding may also have a poor assembly yield if the assembly surface has planarity issues [9].

In an integration scheme for CMOS and MEMS, minimization of the thermomechanical stress in MEMS chips is an important issue that must be addressed, as many MEMS devices are sensitive to such stress. For example in one study, the performance of a MEMS device was changed as much as 37% as a result of the thermomechanical stress [6]. In another study, a piezoelectric MEMS device was even used to quantify the thermomechanical stress experienced by the MEMS chip [7].

The 3D integration of CMOS and MEMS has a great potential to address the process complexity issue of monolithic integration, as well as the performance issue of the package-based integration. By fabricating CMOS IC and MEMS chip independently, assembling them on top of each other and making vertical interconnections, MEMS designers are no longer restricted to a narrow process window available with monolithic integration, nor the low performance routing and redistribution wires used in a package-based integration.

Also, by making the vertical interconnections using Mechanically Flexible Interconnects (MFIs) as shown in Figure 3, it is also possible to address the problem of thermomechanical stress. MFIs are discussed in the first part of the paper.

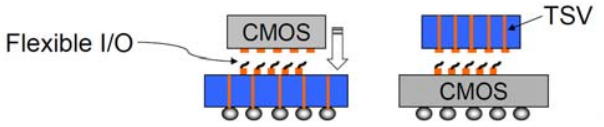


Figure 3. 3D integration of CMOS and MEMS using MFIs and TSVs.

Despite the advantages that 3D integration can offer, however, it does introduce one additional complexity; in order to expose the MEMS/sensor to the environment, a back-to-face 3D integration is needed which requires devices on the face of the chip to make interconnections to the backside of the chip – a Through Silicon Via (TSV) technology is needed for a 3D integration of CMOS and MEMS (Figure 1). The second part of the paper will discuss a new TSV technology specifically designed for this purpose.

## III. Mechanically Flexible Interconnects

Flexible interconnects' ability to reduce thermomechanical stress has been demonstrated before [1, 10-13], and if it is used correctly between MEMS and package substrate, it can significantly reduce the thermomechanical stress from propagating to MEMS devices. If needed, flexible interconnects can also be used between CMOS ICs and the package substrate to reduce thermomechanical stress in CMOS ICs as well.

Flexible interconnects like MFIs also have other potential benefits; it can be used to make low-force and low-resistance temporary electrical connections with a bare-die, enabling at-speed testing of chips before they are bonded to the final substrate [10, 14, 15]. It can also be used to make disposable sensor system where only the potentially contaminated sensor chip is replaced while the "expensive" CMOS IC is reused [16, 17]. MFIs can also allow assembly of chips that may not have a perfectly planar surface; by applying sufficient load during the assembly and MFIs can even make contact to surfaces inside a cavity or surfaces on top of a tall feature.

However, in order to use MFIs for such purposes in addition to using it to reduce thermomechanical stress, it is essential that MFIs can take advantage of most of the vertical standoff height without being damaged or going through a significant plastic deformation, which could reduce the available standoff height and degrade the capability of MFIs.

### A. Tapered Interconnect Structure

In order to minimize the plastic deformation of the flexible interconnect structure during vertical deformation, a tapered interconnect design was used instead of a more common constant width design; by linearly varying the width of the

beam, it is possible to distribute the stress more uniformly [18]. This lowers the maximum stress experienced by the beam as shown in the ANSYS simulation (Figure 4).

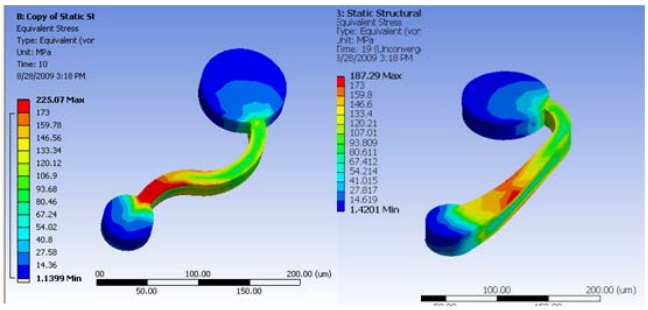

Figure 4. Mechanical FEM simulation using ANSYS shows less maximum stress in a tapered interconnect structure (right) compared to a constant width structure (left).

## B. Curved Beam Design

In order to allow the 100% of the stand-off height to be utilized, it was also necessary to diverge from the conventional cantilever design as shown in Figure 5. With such design, the range-of-movement would be restricted to the height of material deposited on the tip of the beam, which in this case was the height of the solder ball. By having a curved beam design as shown in Figure 5, this problem can be avoided and it is the design used for the MFIs in this paper (Figure 6). This design is especially critical if the interconnect pitch is to be scaled down while the vertical standoff height is kept constant.

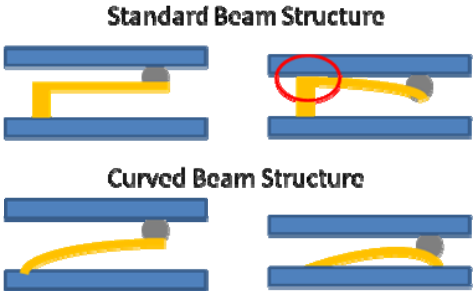


Figure 5. Conventional beam (top) and curved beam (bottom) under loading. Conventional beam design has a limited vertical range of motion due to the vertical post.

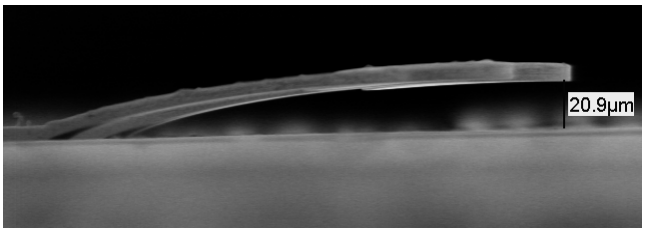


Figure 6. SEM of an MFI from the side showing its curved beam structure.

## C. Solder Confinement

If eutectic bonding using solder is to be used as the bonding mechanism, it was also necessary to devise a method to prevent solder from wetting the entire interconnect structure as it would cause unexpected mechanical behavior and therefore inconsistent assembly results. A polymer ring was formed on the pad area as shown in Figure 7b, and the solder was deposited in the middle (Figure 7c). Figure 7 shows that solder is confined to the pad area only after reflowing. The polymer rings also allow electroplating of various UBM metals underneath the solder; in this work, nickel used as an UBM .

Apart from eutectic bonding, alternative methods of bonding are currently being investigated including various copper to copper bonding technologies.

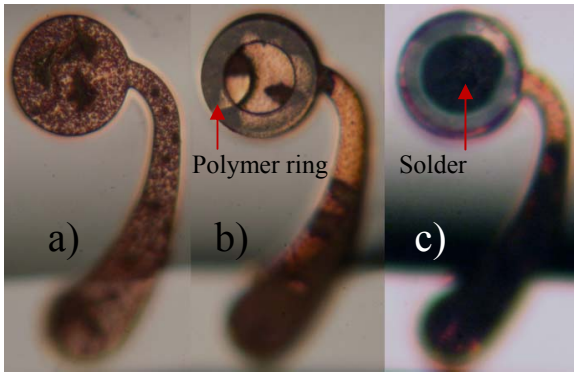


Figure 7. a) MFI b) MFI with a polymer ring c) MFI with polymer ring and solder ball

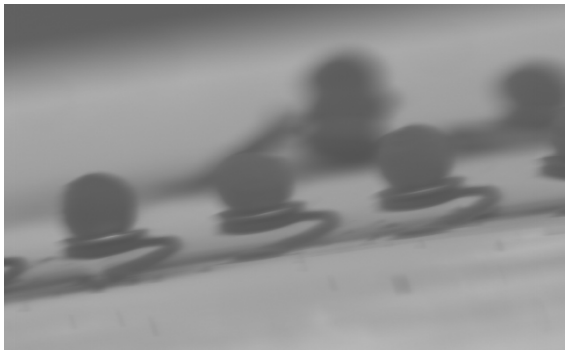

Figure 8. MFIs after solder reflow.

## D. Fabrication

The process flow for fabricating MFIs is shown in Figure 9. The process can be performed at the wafer level and are processes that can be implemented following the end of the semiconductor back-end-of-the-line (BEOL) processes. This allows MFIs to be fabricated on a CMOS chip as shown in Figure 1.

The first part of the process is the fabrication of the curved polymer surface. This is done by spin coating a photodefinable sacrificial polymer and then reflowing it (Figure 10). Though the shape of the curved polymer surface is created almost instantly, the reflowed polymer then needs to be cured at 150°C in order to increase the glass transition temperature ($T_g$) and to remove excess solvent [19].

Increasing the glass transition temperature of the polymer is critical, as initial glass transition temperature is below many of the baking temperatures of the photoresists used in following processes. The optimal curing time and temperature were experimentally determined.

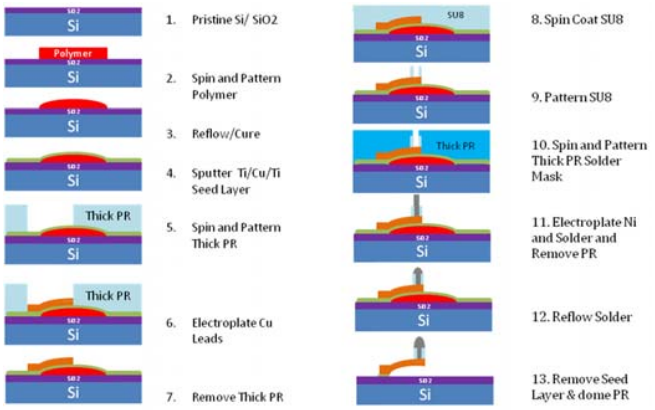

Figure 9. MFI fabrication process.

The second part of the process is to deposit an electroplating seed layer on top of the reflowed polymer. For the seed layer, 300 angstrom of titanium, 2000 angstrom of copper and 300 angstrom of titanium is deposited using a DC sputter. Titanium was used as an adhesion promoter.

The third part of the process is to spin coat and pattern an electroplating mold for the electroplating of the interconnect beam structure. After the mold formation, the wafer is dipped in Buffered Oxide Etch (BOE) to remove the top Ti layer exposing the copper layer. Copper is then electroplated in a copper sulfate based solution.

Figure 10. Curved polymer surface fabrication.

After electroplating the copper, the electroplating mold is removed. SU8 polymer ring is then formed and another electroplating mold with an opening inside the polymer ring is formed. Nickel and solder are then electroplated respectively.

Finally, the seed layer is removed followed by the removal of the sacrificial polymer (using acetone), which releases the MFIs.

Using the above process, MFIs as small as 100µm x 50µm have been successfully fabricated at the wafer (4") level (Figure 11).

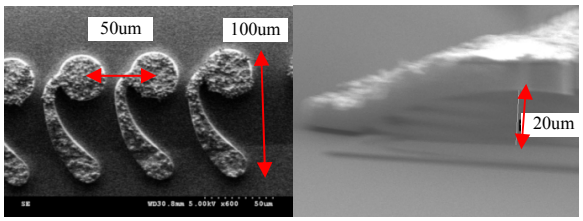

Figure 11. 100µm x 50µm pitched MFIs.

## E. Mechanical Simulations

Compliance of the MFIs was simulated using a FEM software package (ANSYS). The interconnect structure was modeled as a linear elastic model with copper material properties; Young's modulus of 121 GPa and Poisson's ratio of 0.36 were used. Solder ball and polymer ring were omitted from the simulation for simplicity and under the assumption that their presence does not change the mechanical behavior significantly.

The structure was completely constrained on one side and the force was applied in the middle of the round pad area. Compliance was calculated by dividing the z-directional displacement by the applied force.

For determining compliance, there are two cases to consider; the first case is when the tip of the beam is completely free and the second case is when the tip of the beam is guided i.e. in-plane translation and rotation degree of freedom at the tip of the beam is fixed.

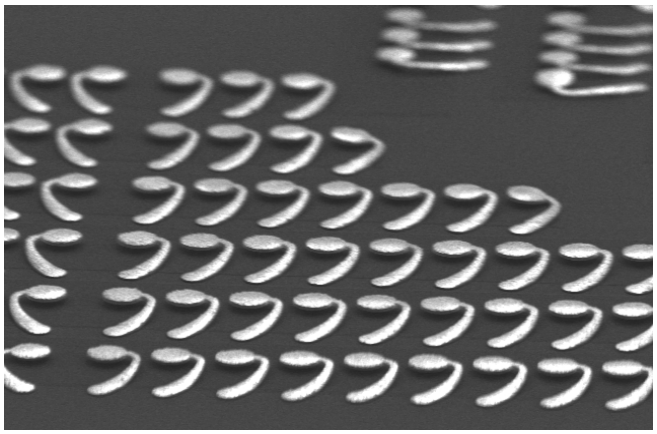
Figure 12. Area array of MFIs.

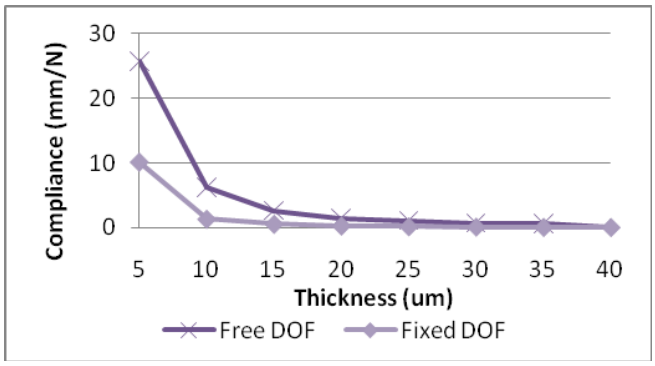

Figure 13. Compliance of the MFIs with varying thicknesses.

The first case approximately simulates the case of the interconnect structure during the assembly when the solder is being reflowed and not yet solidified, while the second case approximately simulates post-assembly process when the solder has solidified and the in-plane translation and rotation is restricted as the beam structure is deformed vertically.

Results of the simulations are shown in Figure 13. It is evident from the simulations that by fixing the rotational degree of freedom (DOF) and in-plane translation at the tip of the beam structure, the compliance is reduced. This suggests that less compliance is available once the chip is assembled compared to the compliance available during the assembly process. Stress experienced by the beam for the guided case

was also higher than the free case indicating that the plastic deformation of the structure will occur at lower degree of deformation for the guided case.

F. Mechanical Characterizations

To determine the vertical compliance, indentation experiments were carried out using a Hysitron Triboindenter. Ten 12µm thick 200µm x 100µm MFIs from a 4in wafer were selected at random and were indented vertically. Triangular load profile with a peak load of 1000uN was applied. The average compliance was 4.25 mm/N with a standard deviation of 0.337. The simulation's predicted compliance was 4.5mm/N.

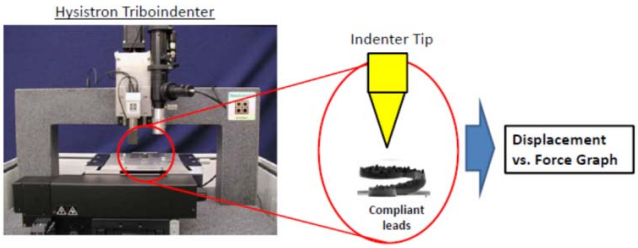


Figure 14. Indentation experiment setup.

In order to determine the extent of plastic deformation, a single 12µm thick 200µm x 100µm MFI was indented multiple times. The maximum vertical displacement achieved was 4µm, which was limit of the equipment used. Results show no sign of plastic deformation as both the loading and unloading curves were an identical linear curve as shown in Figure 15. Even after the twentieth indentation, the loading and unloading curves were matched and identical to the first indentation.

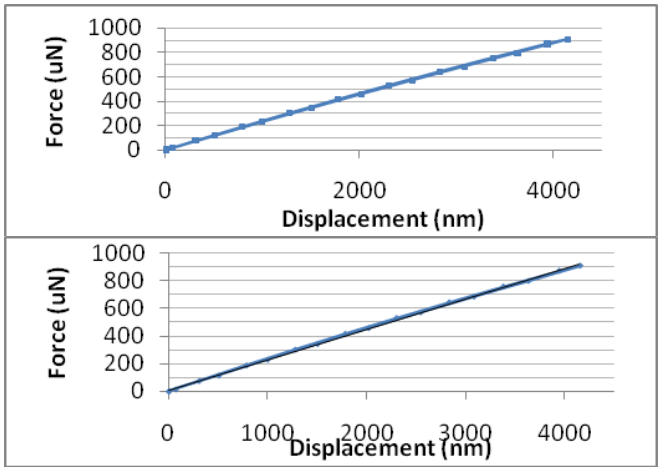


Figure 15. Force vs. Displacement of 12µm thick MFI a) first indentation b) after twenty indentations. It has a linear loading and unloading profile that is matched meaning that no plastic deformation has occurred.

Although no discernable plastic deformation occurred for less than 4µm of vertical displacement, it was necessary to determine the extent of plastic deformation when the MFIs were fully deformed vertically. Similar to the simulation, two cases, free tip case and guided tip case, were approximately emulated.

In order to approximate the free tip case, the indentation was performed at the outer most point of the pad area (Figure 16). For the guided tip case, the indentation was performed at the inner most part of the pad area to approximate the inward pad rotation; at maximum displacement, the pad was pressed flat against the substrate. Unfortunately, there was no way to fix the X, Y translation of the pad area.

After the indentation, the samples were examined under an SEM, and its new standoff height measured. The new standoff heights after the indentations are tabulated in Table 1.

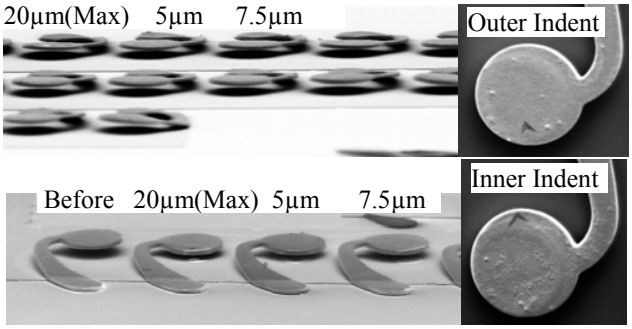


Figure 16. Free tip case (top) and guided tip case emulation (bottom).

| | *5µm* | *7.5µm* | *20 µm* |
|---|---|---|---|
| **Inner Indent** | 20µm | 18µm | 15µm |
| **Outer Indent** | 20µm | 20µm | 20µm |

Table 1. Standoff height after indentation.

For the "free tip" case, there was no discernable change in the stand-off height, while the "guided tip" case showed visible yielding beyond 5µm of vertical displacement. This result is not surprising as ANSYS simulations in previous section showed higher stress for the "guided tip" case. Still, this is an important result as 15µm of standoff height was still available after the being pressed flat against the substrate.

It is important to remember, however, that the compliance of the interconnect structure is not limited to less than 4mm/N; as shown from simulations, by adjusting the thickness of the beam, compliance can be raised up to 25mm/N to fit requirement of the application. Future work will involve optimization of MFI thickness, materials, and geometry as well as additional mechanical characterizations.

G. Assembly

From the mechanical simulations, the available compliance of a single MFI during the assembly process is 4.5mm/N. The test chip contained 424 MFIs and as a result the compliance of an array of MFIs is 0.011mm/N. At room temperature, at least 1.8N of pressure must be applied for MFIs to deform 20µm vertically; this is critical if one is trying to compensate for surface non-planarity of up to 20µm. Hence, 200g was applied to the top of the chip during the assembly process. The temperature profile used for the assembly is shown in Figure 17.

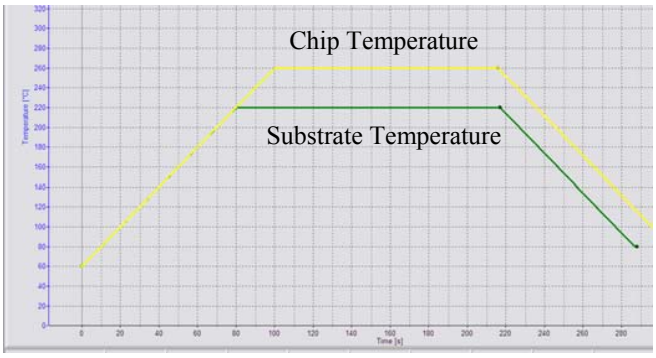

Figure 17. Assembly temperature profile.

After the assembly process, the chip was separated from the substrate in order to test the bond strength of the solder to the pad. The Figure 18 shows that all of the MFIs transferred to the chip indicating that the bonding strength is better than the bonding strength of sputtered copper to silicon dioxide. These figures also shows that the polymer ring is unaffected by the assembly process with temperature elevated up to 260°C. Future work includes more critical testing of the assembly process (electrical and mechanical).

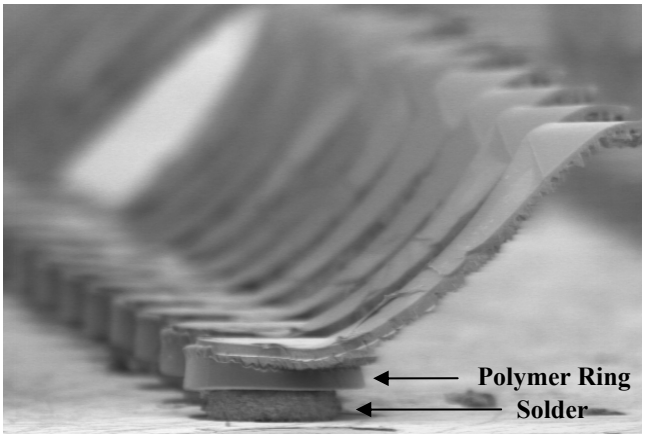

Figure 18. Side view of "peeled off" MFIs after assembly.

## IV. Through Silicon Vias (TSV)

TSV requirement for MEMS chips may be different from TSV requirement for CMOS ICs. First, unlike CMOS ICs which can be thinned down to tens of microns, MEMS chips cannot be thinned down as aggressively, in general. This is because some MEMS devices are hundreds of microns deep or because thinning of the wafer can cause severe chip bending which affect the performance of the MEMS. Unfortunately, many of the TSV technologies that have been developed and are being researched exploit the fact that the chips are thinned down prior to the TSV fabrication.

Also, if TSV technology is to be fabricated after the MEMS/sensor devices, then the fabrication process for TSV should not be damaging to often sensitive MEMS devices. Specifically, the Chemical-Mechanical Planarization (CMP), which is often used for planarizing conductors filled using electroplating technique, should be avoided as it may damage significant number of MEMS devices. Presently, however, electroplating is a popular via filling technique for thick wafer TSVs [20].

The TSV technology presented in this paper includes a technique that does not require CMP on the device side of the wafer and its fabrication has been demonstrated at 8:1 aspect ratio with 50µm vias on a 400µm thick wafer [21]. However, this was limited by the DRIE tool that was available at the lab; with a newer DRIE tools, the same technique can be used to fabricate higher aspect ratio TSVs.

The fabrication process for TSVs begin with a PECVD deposition of $SiO_2$ on the sensor side of the wafer. Then, DRIE tool was used to etch a through via hole in the wafer from the backside, using the $SiO_2$ as the stop layer.

After via holes have been etched, a 3um mesh pattern, as shown in Figure 20a, is patterned on the suspended $SiO_2$ using an RIE. Then, seed layer for electroplating is deposited using an e-beam evaporator. E-beam evaporator is used to avoid deposition of the metal on the sidewalls of via holes which can cause non-uniform electroplating leading to formation of voids.

Then, with the back side covered using a non-conductive tape, the wafer is electroplated in copper sulfate based electroplating solution until the mesh pattern is closed, or "pinched off", as shown in Figure 20b.

The non-conductive tape is now placed on the sensor side of the wafer and then the back side is now electroplated. First, nickel is electroplated. Then, copper is electroplated until the vias are completely filled up as shown in the Figure 21c. Pulsed current with an on duration of 4.5ms and an off duration of 9ms was used for electroplating.

Excess copper on the wafers are removed in two different ways. For the device side, acid based copper etchant is used, which can selectively remove the excess copper in matter of minutes. Due to the presence of electroplated nickel, only the excess copper on the sensor side is removed while the electroplated copper inside the via hole is unaffected. For the backside, a CMP is used to planarize and remove excess copper. Cross-section of TSVs in Figure 20c shows that despite the use of mesh seed layer, no voids are formed.

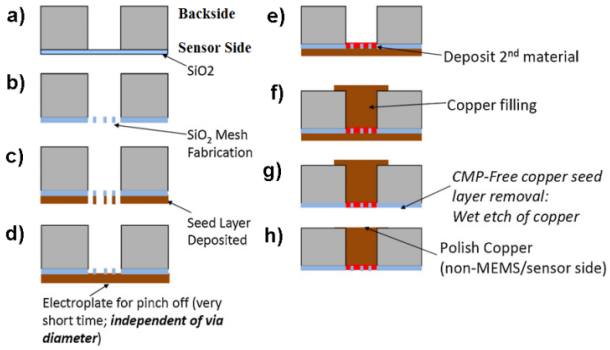

Figure 19. TSV fabrication process.

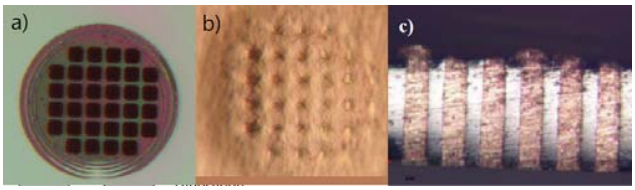

Figure 20. a) TSV with 3um mesh membrane suspended on top of a 50um diameter via hole b) mesh after "pinch off" c) cross sectional image showing that TSVs are filled without voids.

## V. Conclusions

MEMS/sensor industry is projected to grow very rapidly in the next decade. With its growth, the number of MEMS devices will be growing rapidly as well. As a result, an integration scheme that allows an arbitrary MEMS device to be integrated with CMOS is desirable.

In this work, we present such technology consisting of MFIs and TSVs. By vertically integrating CMOS and MEMS using MFIs, independent fabrication of CMOS ICs and MEMS chips as well as high density and high performance interconnections can be achieved while TSVs allow devices and sensors to be exposed to the environment.

**Acknowledgments**

This work has been carried in part under a Semiconductor Research Company (SRC) GRC Project 13066P8. Special thanks to project mentors Masood Mutuza and Mario Bolanos-Avila at Texas Instruments (TI) and Eric Luckowski at Freescale.

**References**

[1] M. Bakir and J. Meindl (Eds.), Integrated Interconnect Technologies for 3D Nanoelectronic Systems, Artech House (Massachusetts, 2009).

[2] T. F. Marinis, "The future of Microelectromechanical Systems (MEMS)," *Strain*, Vol. 45, No.3 (2008), pp208-220.

[3] A. Witvrouw, "CMOS-MEMS Integration: Why, How and What?" *IEEE/ACM International Conference on Computer-Aided Design,* Nov. 2006, pp.826-827.

[4] H. Baltes, O. Brand, G. K. Fedder and C. Hierold, CMOS-MEMS: Advanced Micro and Nanosystems, Wiley-VCH (2005).

[5] A. J. Joseph *et al.*, "Through-silicon vias enable next-generation SiGe power amplifiers for wireless communications," IBM Journal of Research and Development, Vol. 52, No. 6 (2008), pp.635-648.

[6] M. Lishchynska, C. O'Mahony, O. Slattery, O. Wittler and H. Walter, "Evaluation of Packaging Effect on MEMS Performance: Simulation and Experimental Study," *IEEE Tran-Advanced Packaging*, Vol.30, No.4 (2007), pp.629-635.

[7] D. Pustan, E. Rastiagaev and J. Wilde, "In situ analysis of the stress development during fabrication processes of micro-assemblies," *Proc. IEEE 59th Electronic Components and Technology Conference*, May 2009, pp.117-124.

[8] Z. Feng, W. Zhang, B. Su; K. C. Gupta and Y. C. Lee, "RF and mechanical characterization of flip-chip interconnects in CPW circuits with underfill," *IEEE MTT-S International Microwave Symposium Digest*, Vol.3 (1998), pp.1823-1826.

[9] N. Basavanhally *et al*, "High-Density Solder Bump Interconnect for MEMS Hybrid Integration," *Advanced Packaging, IEEE Transactions on*, Vol. 30, 2007, pp. 622-628.

[10] E. M. Chow, D. De Bruyker, I. Shubin, J. Cunningham, B. Cheng, K. Sahasrabuddhe, Y. Luo and J. Simons, "Microspring characterization and flip chip assembly reliability," *42nd International Symposium on Microelectronics (IMAPS)*, San Jose, CA, Nov. 2009.

[11] Q. Zhu, L. Ma and S. K. Sitaraman, "β-Helix: A lithography-Based Compliant Off-Chip Interconnect," *IEEE Transactions on Components and Packaging Technologies*, Vol.26, No.3 (2003), pp.582-590.

[12] Q. Zhu, L. Ma and S. K. Sitaraman, "Design Optimization of One-Turn Helix: A Novel Compliant Off-chip Interconnect," *IEEE Transactions on Advanced Packaging,* Vol.26, No.2 (2002), pp.106-112.

[13] M. S. Bakir, H.A. Reed, H.D. Thacker, C.S. Patel, P.A. Kohl, K.P. Martin, and J.D Meindl, "Sea of Leads (SoL) Ultrahigh Density Wafer-Level Chip Input/Output Interconnections for Gigascale Integration (GSI)," *IEEE Transactions on Electron Devices,* vol.50, no.10 (2003) pp.2039-2048.

[14] J. Mitchell *et al.*, "Integrating Novel Packaging Technologies for Large Scale Computer Systems," *Proc. Of InterPACK,* July 2009.

[15] I. Shubin *et al.* "Novel packaging with rematable spring interconnect chips for MCM," *59th Electronic Components and Technology Conference*, San Diego, CA, USA: 2009, pp. 1053-1058.

[16] H. S. Yang, R. Ravindran, M.S. Bakir and J.D. Meindl, "A 3D Interconnect System for Large Biosensor Array and CMOS Signal-Processing IC Integration," *Proc. of IEEE International Interconnect Technology Conference,* Burlingame, CA, June 2010.

[17] R. Ravindran, J. A. Sadie, K. E. Scarberry, H. S. Yang, M. S. Bakir, J. F. McDonald, and J. D. Meindl, "Biochemical Sensing with an Arrayed Silicon Nanowire Platform," *Proc. IEEE 60th Electronic Components and Technology Conference*, June 2010

[18] S.C. Burgess, "The Ranking of Efficiency of Structural Layouts using Form Factors Part 1: Design for Stiffness.," *Proceedings of the Institution of Mechanical Engineers -- Part C -- Journal of Mechanical Engineering Science*, vol. 212, Mar. 1998, pp. 117-128.

[19] J. Sheats and B. Smith, Microlithography Science and Technology, pp. 562, Marcel Dekker Inc. (New York, 1998).

[20] L. Leung and K. Chen "Microwave characterization and modeling of high aspect ratio through-wafer interconnect vias in silicon substrate," *IEEE Trans. Microwave Theory Tech.* Vol.53 (2005) pp.2472–80.

[21] J. Lai, H. S. Yang , H. Chen , C. King , J. Zaveri , R. Ravindran and M. S. Bakir, "A 'mesh' seed layer for improved through-silicon-via fabrication," *Journal of Micromechanics and Microengineering*, Vol. 20, No. 2 (2010).